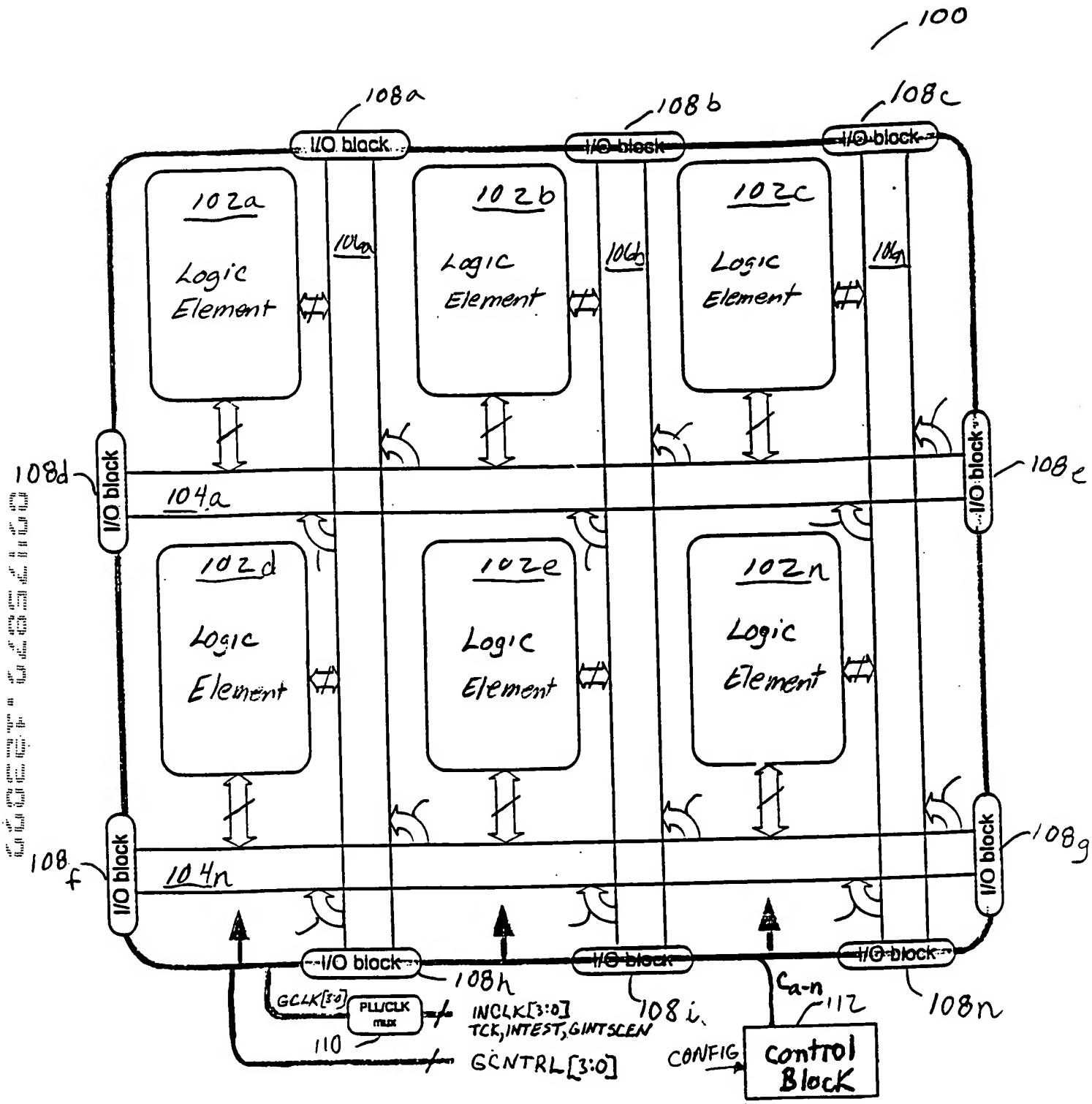
100
108a
108b
108c
I/O block
102a
Logic Element
102b
Logic Element
102c
Logic Element
106a
106b
106n
108d
I/O block
104a
108e
I/O block
102d
Logic Element
102e
Logic Element
102n
Logic Element
108f
I/O block
104n
108g
I/O block
I/O block
108h
I/O block
108i
I/O block
108n
Ca-n
112
GCLK[3:0]
PLL/CLK mux
INCLK[3:0]
TCK, INTEST, GINTSCEN
110
GCNTRL[3:0]
CONFIG
Control Block

FIG.1

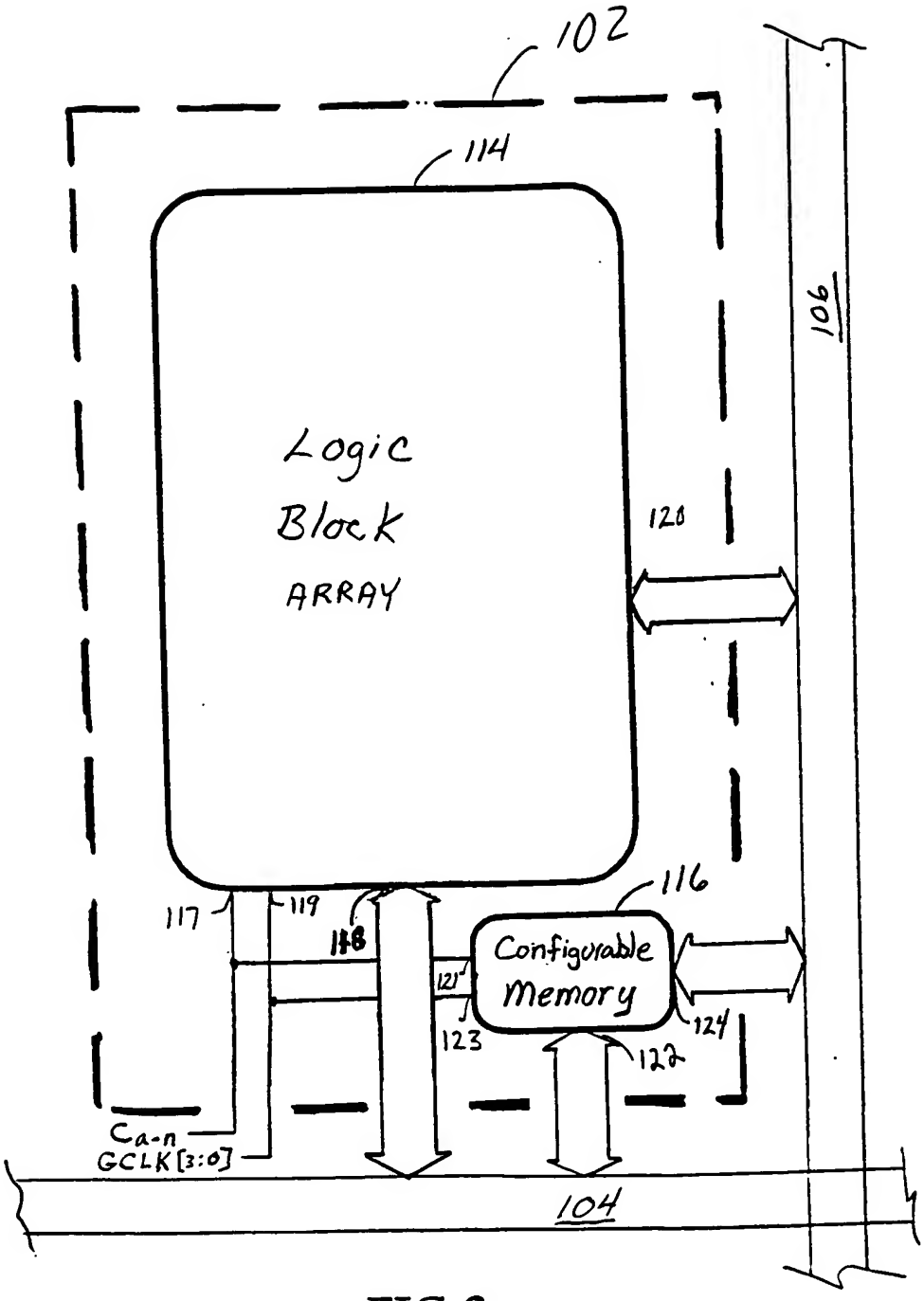
102
114
106
Logic
Block
ARRAY
120
116
Configurable
Memory
117
119
118
121
123
124
122
Ca-n
GCLK[3:0]
104

FIG.2

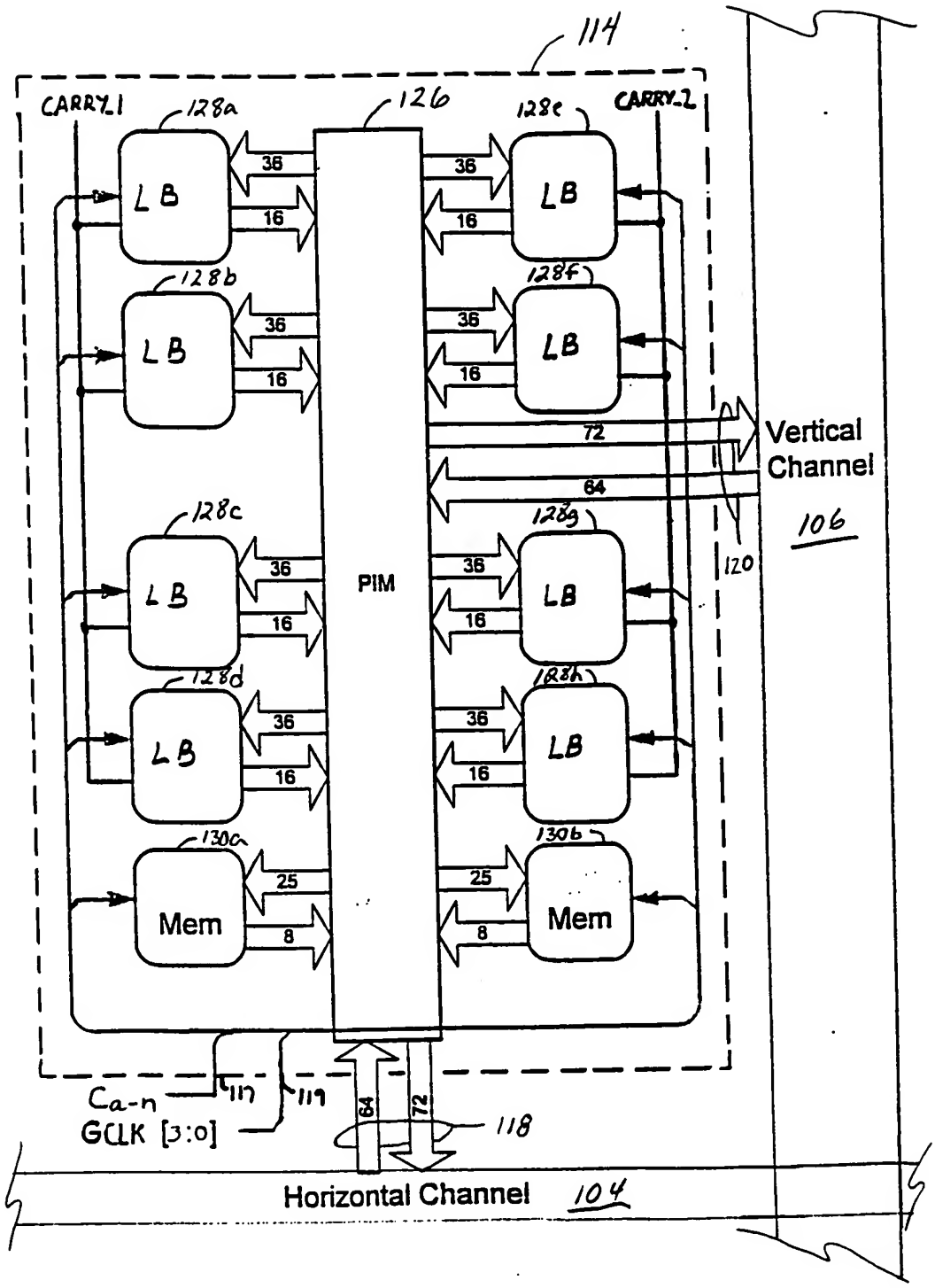
114
CARRY_1
128a
126
128e
CARRY_2
LB
36
16
128b
128f
72
64
Vertical Channel
106
120
128c
128g
PIM
128d
128h
130a
130b
Mem
25
8
Ca-n
GCLK [3:0]
117
119
64
72
118
Horizontal Channel
104

FIG.3

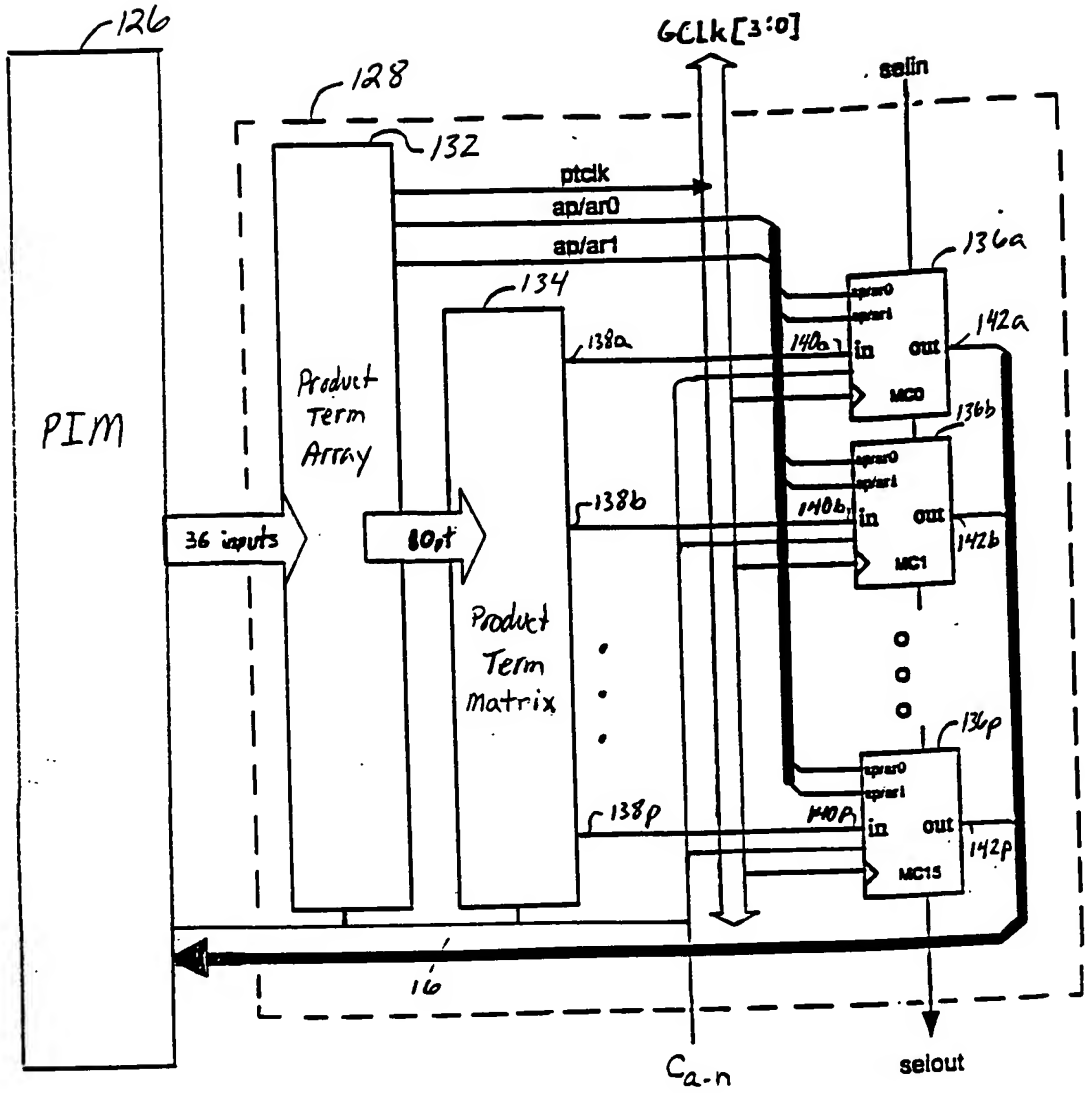
126
PIM
128
132
Product Term Array
36 inputs
80pt
134
Product Term Matrix
GClk[3:0]
selin
ptclk
ap/ar0
ap/ar1
136a
136b
136p
138a
138b
138p
140a
140b
140p
142a
142b
142p
in
out
MC0
MC1
MC15
16
Ca-n
selout

FIG.4

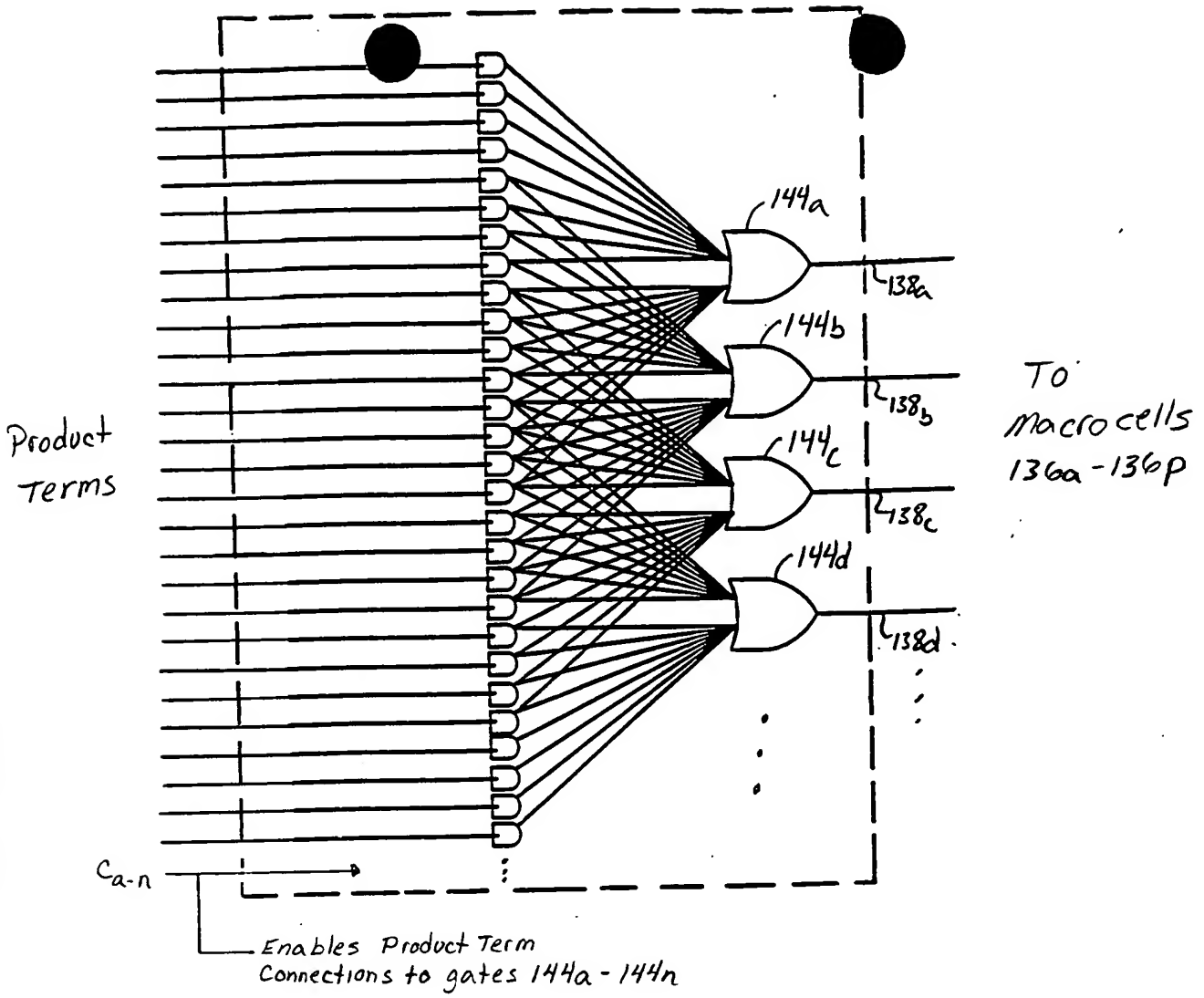
144a
138a
144b
138b
144c
138c
144d
138d
Product Terms
To macrocells 136a-136p
Ca-n
Enables Product Term Connections to gates 144a - 144n

FIG.5

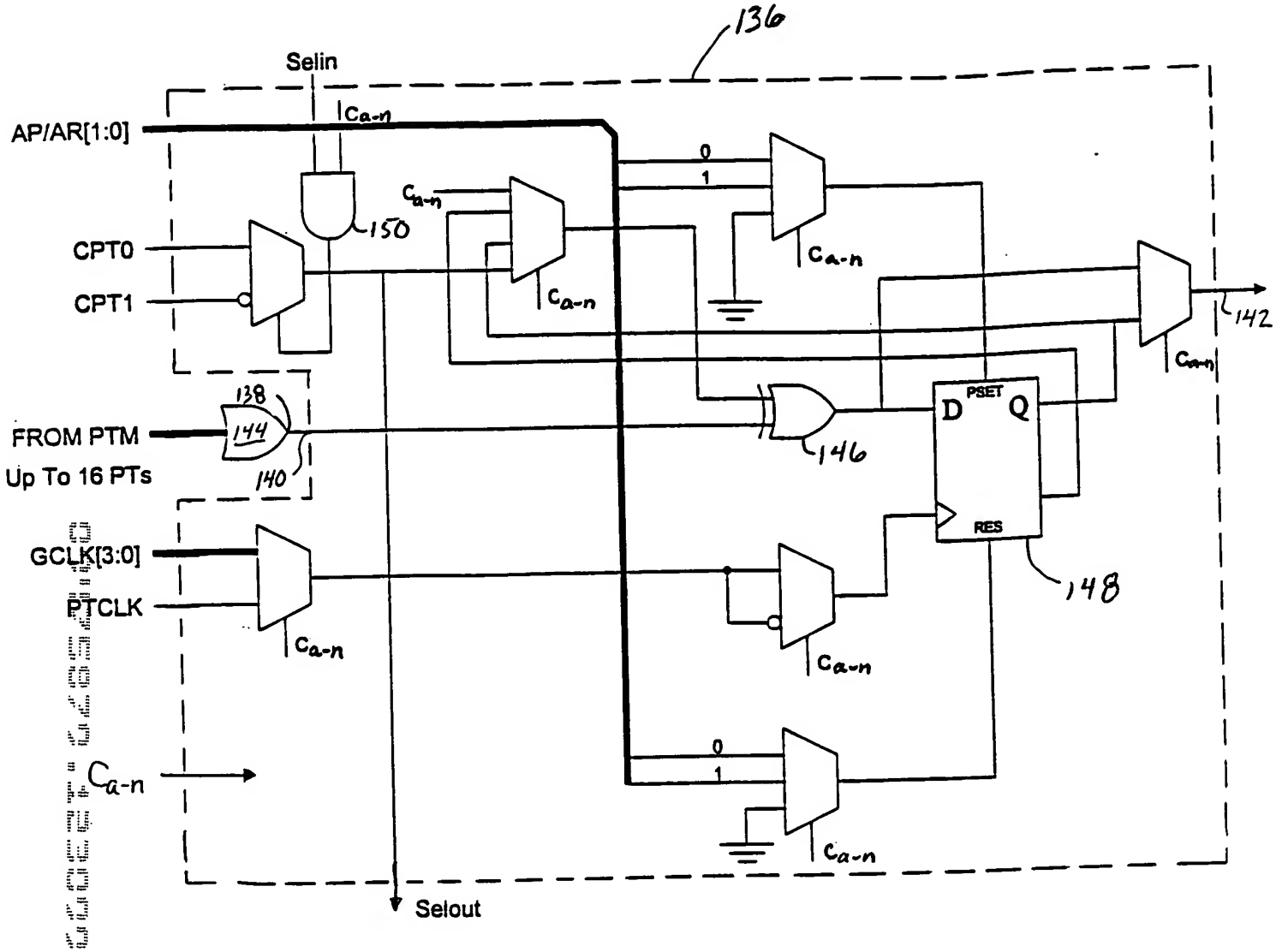
136
Selin
AP/AR[1:0]
Ca-n
150
CPT0
CPT1
0
1
Ca-n
Ca-n
Ca-n
142
138
FROM PTM
Up To 16 PTs
144
140
146
D
PSET
Q
RES
148
GCLK[3:0]
PTCLK
Ca-n
Ca-n
Ca-n
Ca-n
Selout

FIG.6

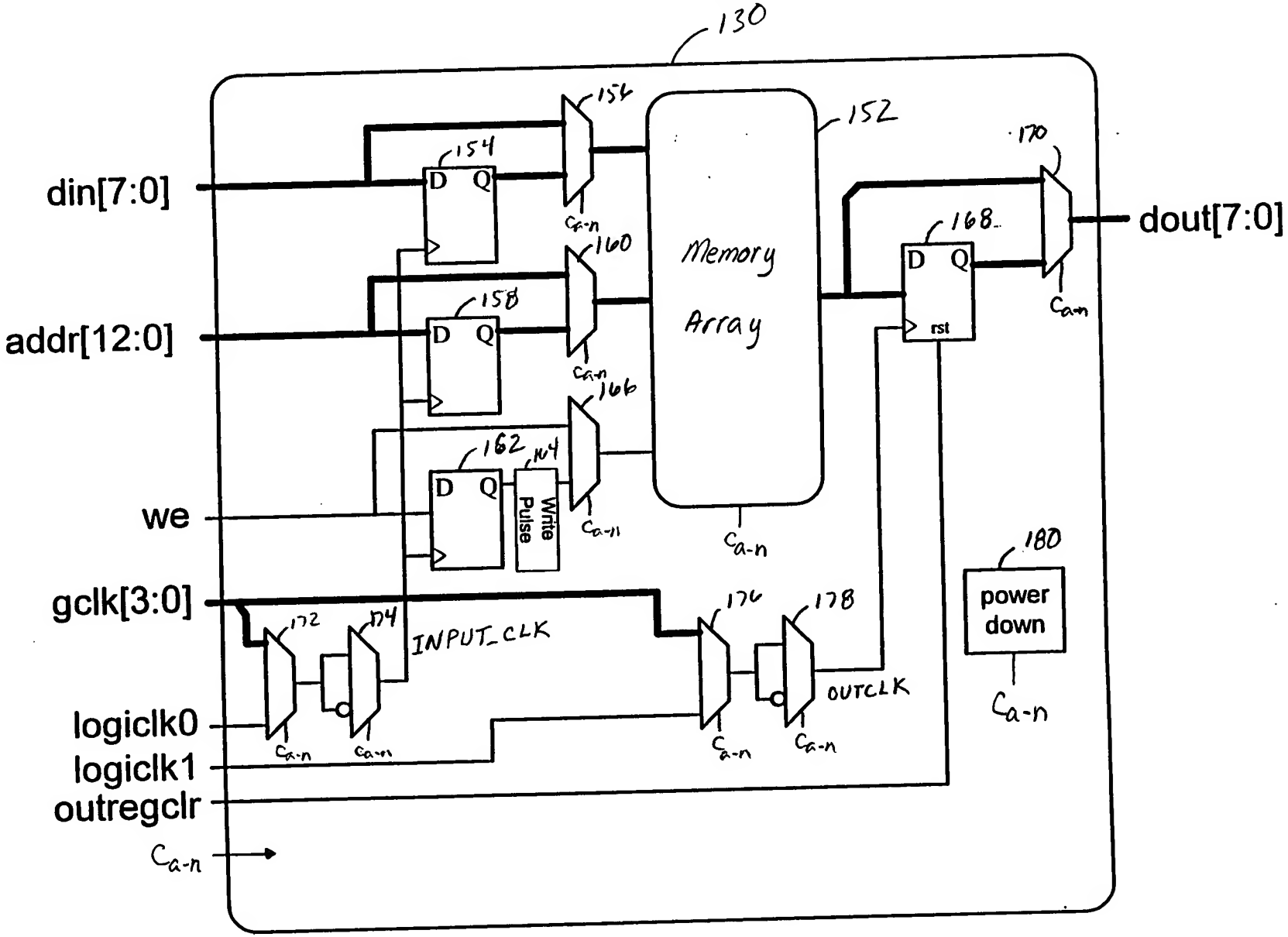
130
154
152
170
din[7:0]
154
D Q
Ca-n
Memory
Array
dout[7:0]
168
D Q
160
addr[12:0]
158
D Q
Ca-n
rst
Ca-n
166
162
164
D Q
Write
Pulse
we
Ca-n
Ca-n
180
power
down
gclk[3:0]
172
174
INPUT_CLK
176
178
OUTCLK
Ca-n
logiclk0
logiclk1
outregclr
Ca-n

FIG.7

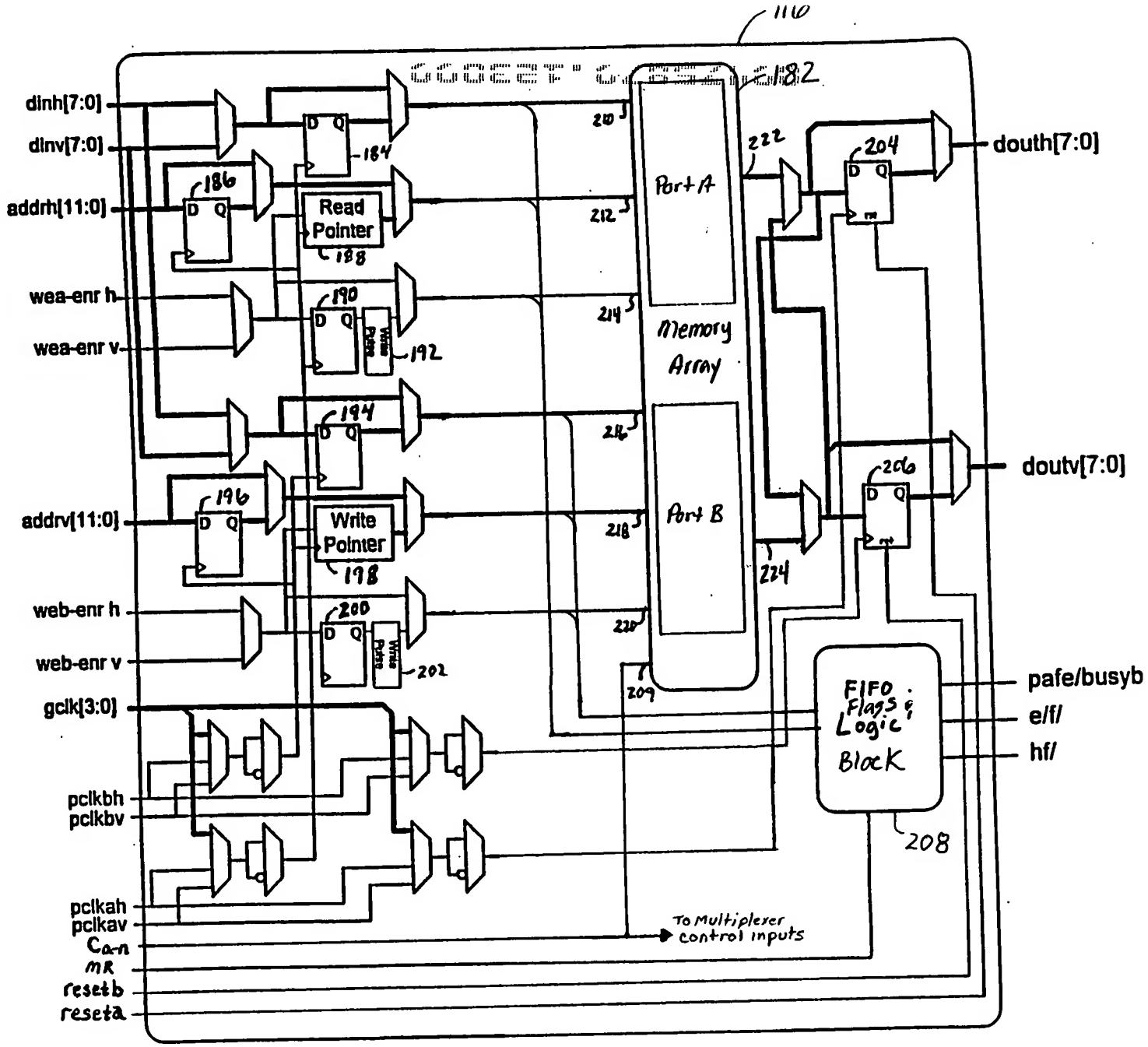
110
182
dinh[7:0]
dinv[7:0]
addrh[11:0]
wea-enr h
wea-enr v
addrv[11:0]
web-enr h
web-enr v
gclk[3:0]
pclkbh
pclkbv
pclkah
pclkav
Ca-n
MR
resetb
reseta
184
186
Read Pointer
188
190
192
194
196
Write Pointer
198
200
202
210
212
214
216
218
220
209
Port A
Memory Array
Port B
222
224
204
206
douth[7:0]
doutv[7:0]
FIFO Flags & Logic Block
208
pafe/busyb
elfl
hfl
To Multiplexer control inputs

FIG.8

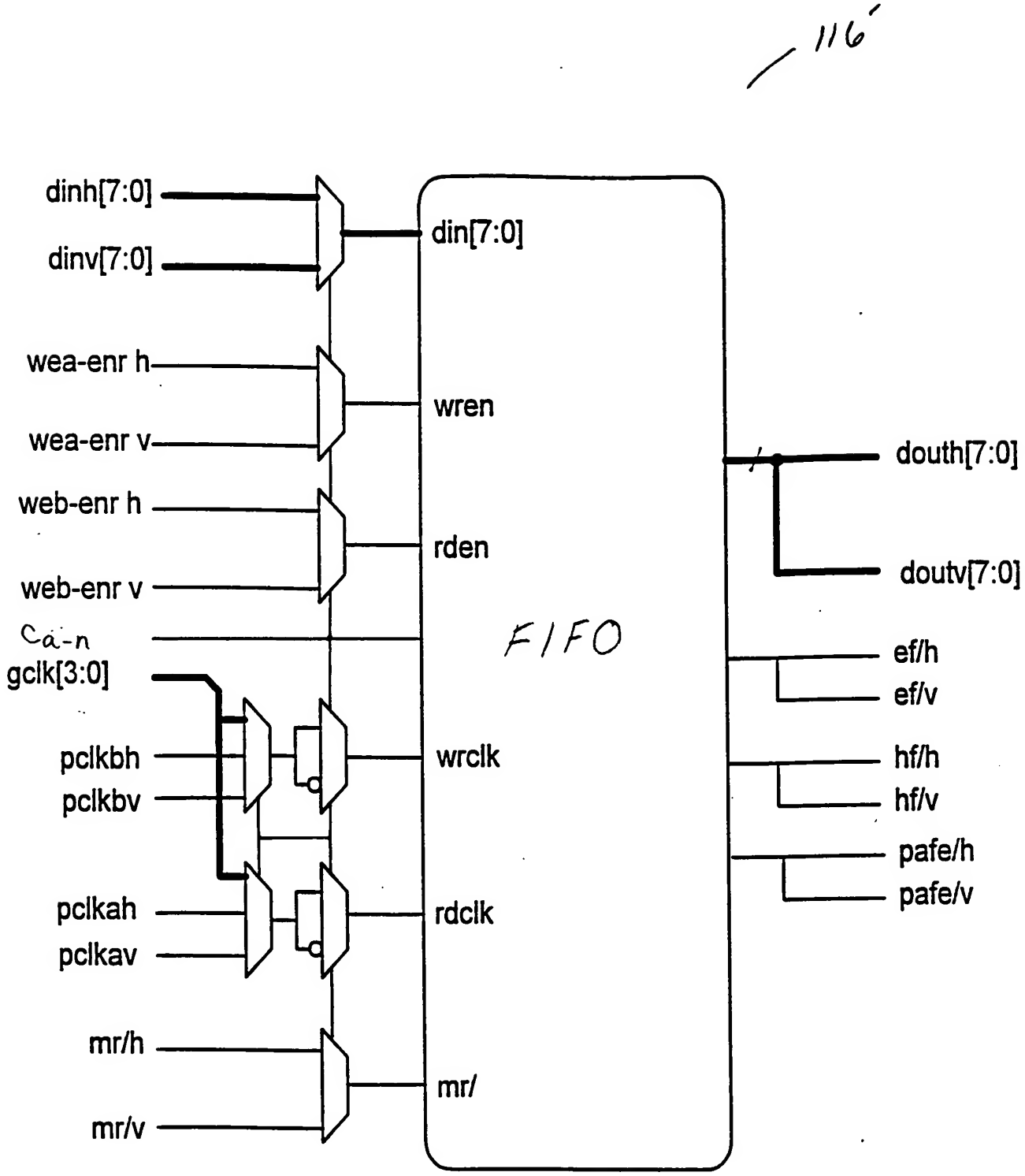
116
dinh[7:0]
dinv[7:0]
din[7:0]
wea-enr h
wea-enr v
wren
douth[7:0]
web-enr h
web-enr v
rden
doutv[7:0]
Ca-n
FIFO
gclk[3:0]
ef/h
ef/v
pclkbh
pclkbv
wrclk
hf/h
hf/v
pafe/h
pafe/v
pclkah
pclkav
rdclk
mr/h
mr/
mr/v

FIG.9

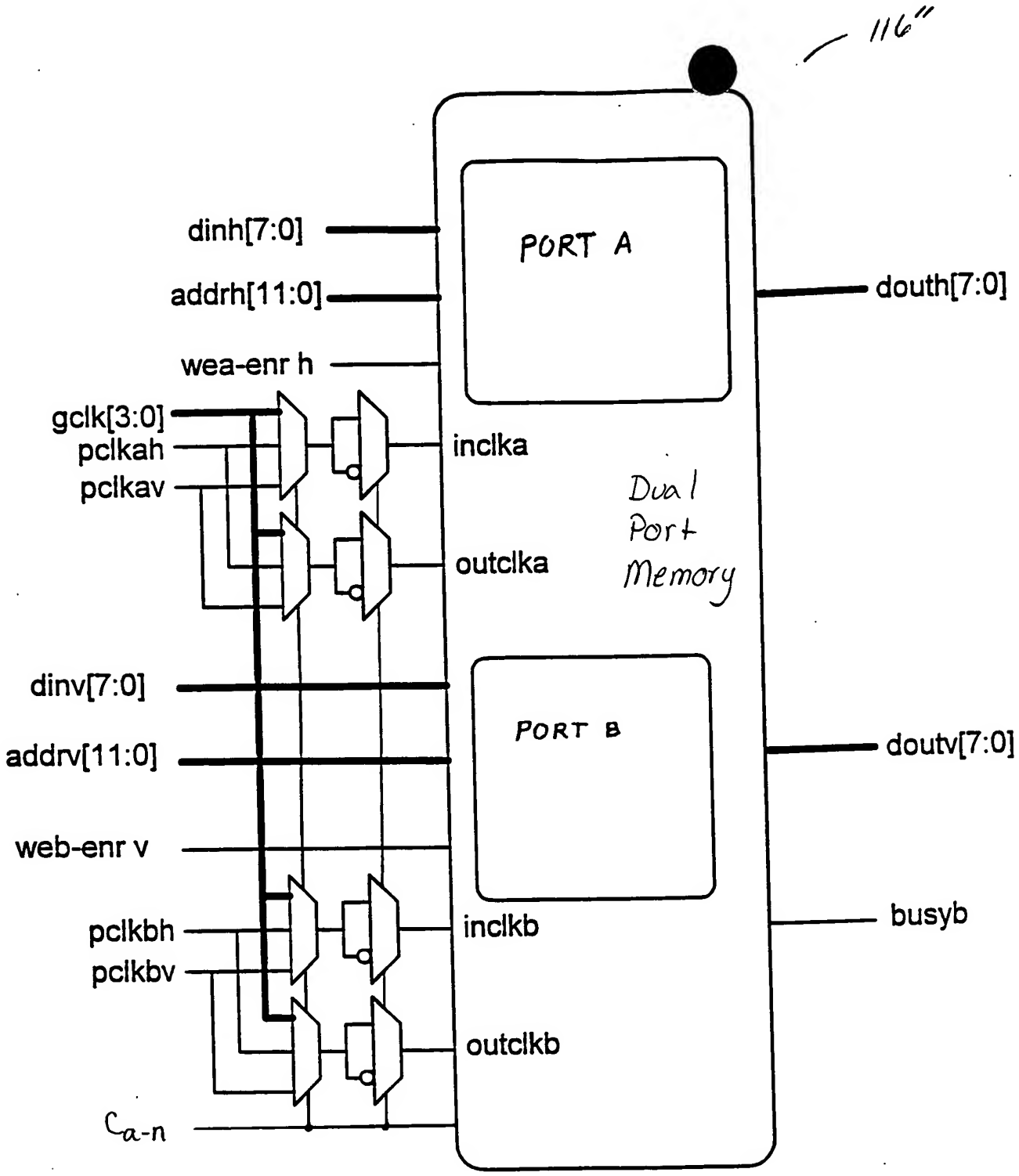
116"
PORT A
PORT B
dinh[7:0]
addrh[11:0]
wea-enr h
gclk[3:0]
pclkah
pclkav
inclka
outclka
Dual Port Memory
dinv[7:0]
addrv[11:0]
web-enr v
pclkbh
pclkbv
inclkb
outclkb
Ca-n
douth[7:0]
doutv[7:0]
busyb

FIG.10

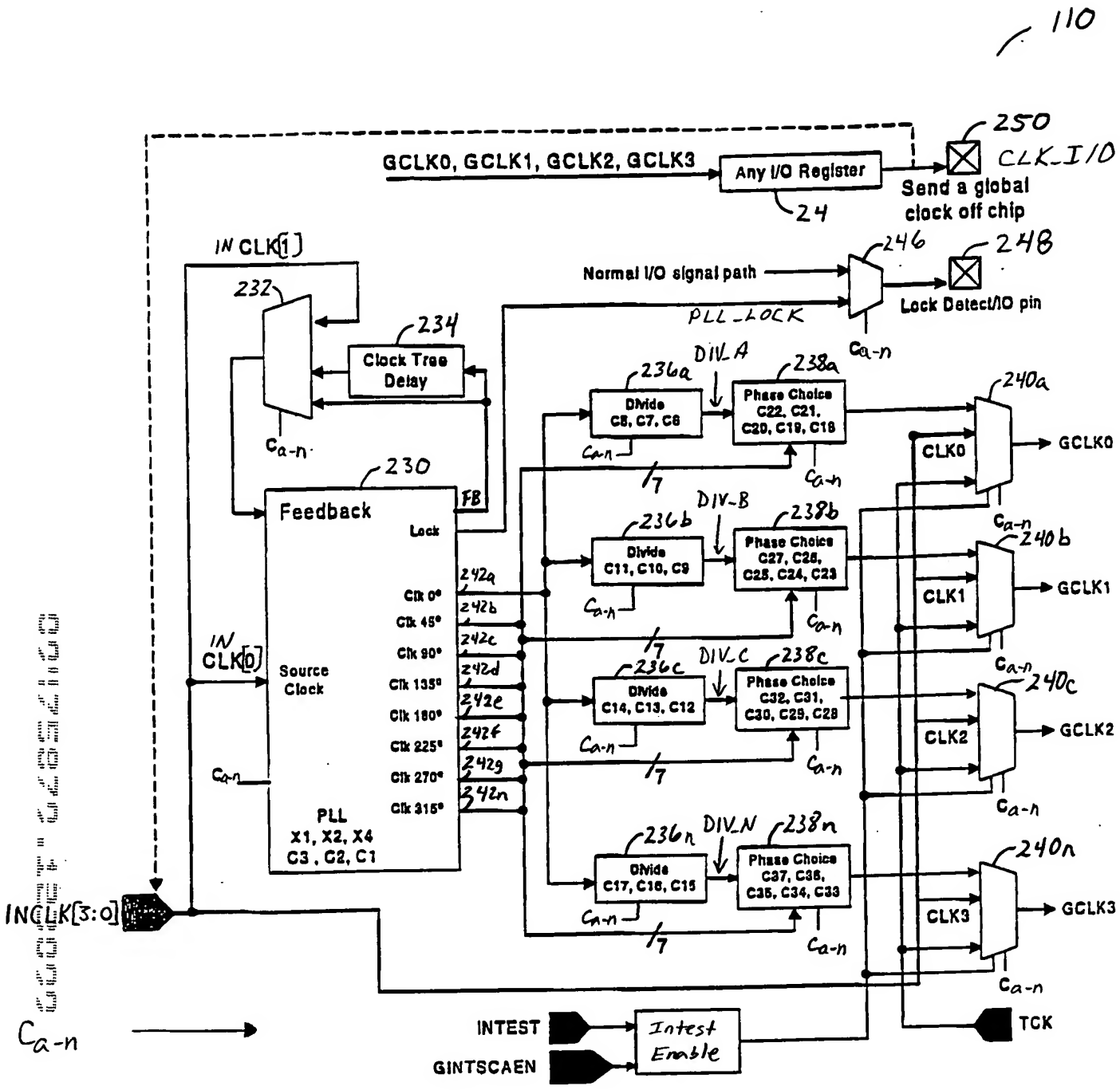
110
250
CLK_I/O
GCLK0, GCLK1, GCLK2, GCLK3
Any I/O Register
24
Send a global clock off chip
IN CLK[1]
246
248
Normal I/O signal path
Lock Detect/IO pin
PLL_LOCK
232
234
Clock Tree Delay
Ca-n
DIV_A
236a
238a
240a
Divide C8, C7, C6
Phase Choice C22, C21, C20, C19, C18
CLK0
GCLK0
230
Feedback
FB
Lock
DIV_B
236b
238b
240b
Divide C11, C10, C9
Phase Choice C27, C26, C25, C24, C23
CLK1
GCLK1
242a
Clk 0°
242b
Clk 45°
242c
Clk 90°
242d
Clk 135°
242e
Clk 180°
242f
Clk 225°
242g
Clk 270°
242n
Clk 315°
IN CLK[0]
Source Clock
DIV_C
236c
238c
240c
Divide C14, C13, C12
Phase Choice C32, C31, C30, C29, C28
CLK2
GCLK2
PLL
X1, X2, X4
C3, C2, C1
DIV_N
236n
238n
240n
Divide C17, C16, C15
Phase Choice C37, C36, C35, C34, C33
CLK3
GCLK3
INCLK[3:0]
INTEST
GINTSCAEN
Intest Enable
TCK

FIG.11

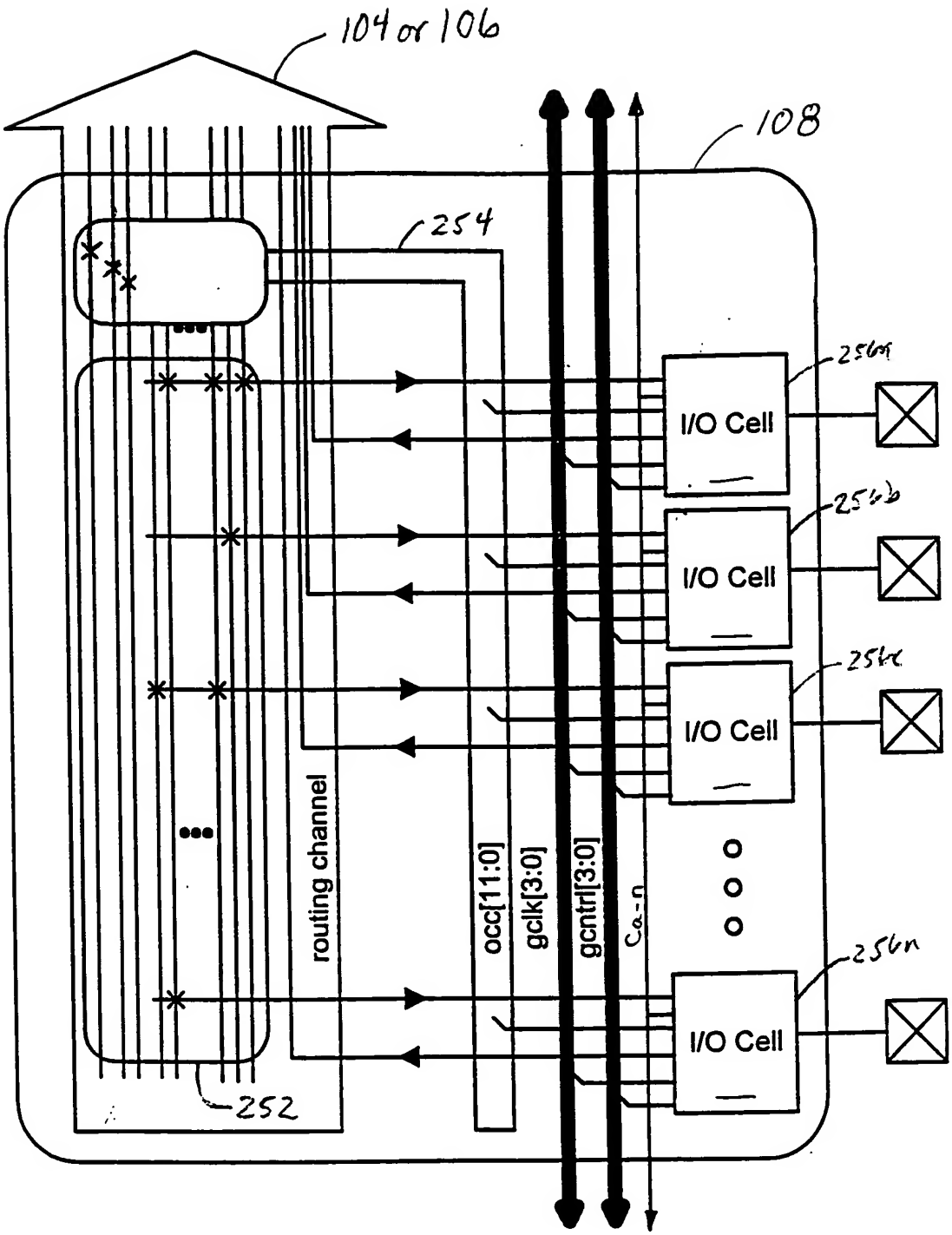
104 or 106
108
254
I/O Cell
I/O Cell
I/O Cell
I/O Cell
routing channel
occ[11:0]
gclk[3:0]
gcntrl[3:0]
252

FIG.12

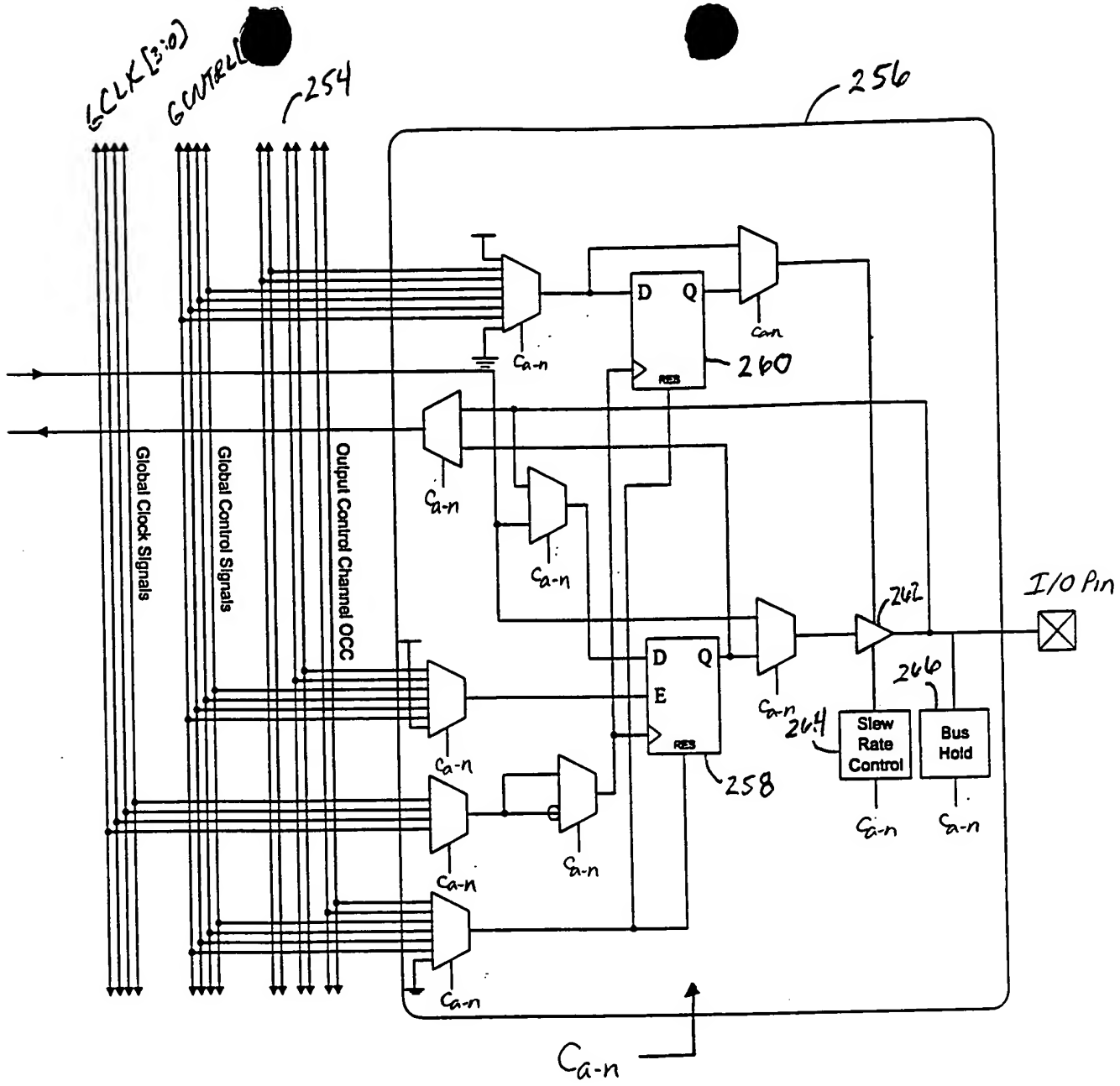
GCLK[3:0]
GCNTRL
254
256
Global Clock Signals
Global Control Signals
Output Control Channel OCC
D
Q
RES
260
Can
Ca-n
I/O Pin
262
266
264
Slew Rate Control
Bus Hold
E
258

FIG.13

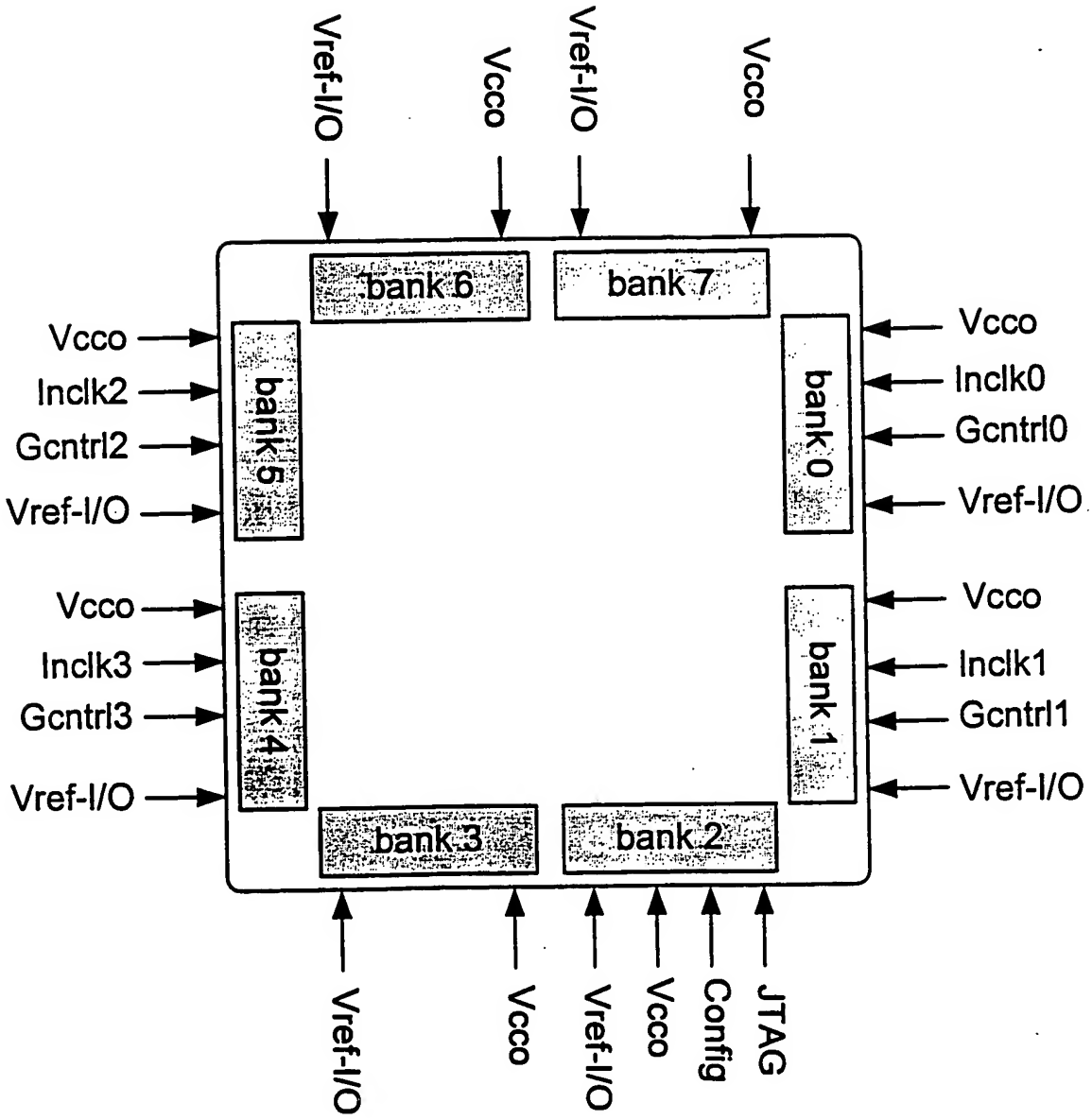
Vref-I/O
Vcco
Vref-I/O
Vcco
bank 6
bank 7
Vcco
Inclk2
Gcntrl2
Vref-I/O
bank 5
bank 0
Vcco
Inclk0
Gcntrl0
Vref-I/O
Vcco
Inclk3
Gcntrl3
Vref-I/O
bank 4
bank 1
Vcco
Inclk1
Gcntrl1
Vref-I/O
bank 3
bank 2
Vref-I/O
Vcco
Vref-I/O
Vcco
Config
JTAG

FIG.14